REMARKS

This paper is responsive to the official action dated July 23, 2003. At the time of the official action, claims 1-34 were pending in the application. All pending claims 1-34 were rejected. The following issues raised by the Office are addressed below: I) the drawings were objected to as failing to comply with 37 C.F.R. §1.84(p)(4); II) claims 13 and 17 were objected to because of informalities; III) claims 1-22, 26-31 and 34 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212,599 issued to Baweja, et al. (Baweja); IV) claims 32 and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Baweja; V) claims 23-25 were not specifically addressed by the Office, but were identified as rejected on the Office Action Summary.

I) Objection To The Drawings

The Office noted that figure 2 of the application used the same reference numeral, 218, to identify both "AGP CARD" and "HLDSREF#." A replacement sheet for figure 2 has been provided correcting this oversight, and the "AGP CARD" is now identified by reference numeral 226.

In addition to correcting figure 2, the specification has been amended to maintain consistency with the drawings. The amendments to figure 2 and the specification do not introduce any new matter.

II) Objection to Claims 13 and 17

Claim 13

The Office objected to claim 13 because of two apparent informalities: 1) line 2 of claim 13 recites "at at least a first logical level"; and 2) lines 3-4 of claim 13 recite "at a high impedance level." The Office suggests changing the first apparent informality to recite, "to the first logical level," and suggests changing the second apparent informality to recite, "to the high impedance level."

The Applicant respectfully submits that there are no actual informalities in claim 13 that require correction. Although "at at" appears informal, claim 13 is referring to driving the memory control signal at a particular logic level, but allowing for the possibility that the memory control signal may also be driven at more than one level. Hence, the recited wording, "drives the memory control signal at at least a first logic level...," although phrased in an unusual manner, is not incorrectly stated.

Regarding both the first and second apparent informalities, the suggestion by the Office to change the indefinite article "a," as in "a first logic level" and "a high impedance level," to the definite article "the" would be improper, since there is no antecedent basis for "a first logic level" or "a high impedance level" in either claim 13, or claim 1 from which claim 13 depends.

Claim 17

The Office objected to claim 17 due to a misplacement of the word "during." The Applicant has amended claim 17 to correct the informality noted by the Office.

Conclusion regarding objection to claims 13 and 17

In view of the arguments presented regarding claim 13, and in view of the amendments made to claim 17, the Applicant submits that claims 13 and 17 are not objectionable, and respectfully requests the Office to withdraw its objection to these two claims.

III) Rejection of Claims 1-22, 26-31 and 34 under 35 U.S.C. §102(e)

The Office rejected claims 1-22, 26-31 and 35 under 35 U.S.C. §102(e) as being anticipated by Baweja. For the reasons set forth below, the Applicant respectfully requests the Office to withdraw its rejection of claims 1-22, 26-31 and 35, and allow these claims to issue.

Independent Claim 1

The Office asserts that Baweja teaches a memory control signal supplied by a first integrated circuit according to an operational state, and controlling the memory control signal from a second memory controller during a power saving state. In support of this position, the Office points to Baweja figure 2. The Office relies on element 260 to show the memory control signal, element 210 to show the first integrated circuit controlling the memory control signal according to an operational state, and element 220 to show the second memory controller that controls the memory control signal during a low power state.

In response to the Office's rejection, the method of claim 1 has been amended to recite,

> *supplying at least one memory control signal to the memory from a first integrated circuit in the computer system according to an operational state, and supplying the memory control signal from another location in the computer system when the computer system is in a power savings state...*

The Applicant respectfully draws the attention of the Office to the fact that first memory controller 210 in figure 2 of Baweja does not supply signal 260 to the memory during either an operational state or a low power state. Based on figure 2 and its description in the specification, it appears that Suspend Memory controller element 220 supplies signal 260 at all times. Thus, Baweja does not teach supplying a memory control signal to the memory from a first IC in the computer system according to an operational state and supplying the memory control signal from another location in the computer system when the computer system is in a power savings state, as required by independent claim 1.

The Applicant submits, therefore, that Baweja does not teach each and every element of independent claim 1, and cannot support a prima facie rejection of claim 1, as amended, under 35 U.S.C. 102(e). Consequently, the Applicant submits that independent claim 1, as amended, is in condition for allowance, and respectfully requests the Office to withdraw its rejection of independent claim 1, and allow claim 1 to issue as amended.

Claim 8

The Applicant believes that claim 8, as originally filed, would have been allowable if written in independent form. The Applicant, therefore, has rewritten claim 8 in independent form, incorporating the limitations of originally filed claim 1.

The Office asserts that figure 2 of Baweja discloses the method recited in claim 1 further comprising isolating the first integrated circuit from the memory during the power savings state. The Office states that the isolating circuit is inherently embedded within the memory system controller 200 in order for the second memory controller 220 to control the memory control signal 260.

While Baweja may disclose removing power from first memory controller 210, Baweja does not disclose isolating first memory controller 210 from memory. The applicant submits that, contrary to the Office's assertion that an isolation circuit is inherent, a circuit to isolate first memory controller 210 is not inherent in figure 2. Baweja does not disclose any reason that isolation would be necessary. The only direct connections from first memory controller 210 to SDRAM 225 shown in figure 2 are SCAS 280 and SRAS 285, which carry signals strobed into SDRAM 225 by HCLK 205 during normal operation (see Baweja, col. 4, lines 41-47). Since HCLK 205 is stopped during a power savings mode (see Baweja, col.4, lines 21-28) there appears to be no need to isolate first memory controller 210. Consequently, no isolation circuit is inherently embedded in memory system controller 200.

The Applicant submits, therefore, that Baweja does not teach each and every element of independent claim 8, inherently or otherwise, and cannot support a prima facie rejection of claim 8 under 35 U.S.C. 102(e). Consequently, the Applicant submits that claim 8 is in condition for allowance, and respectfully requests the Office to withdraw its rejection and allow claim 8 to issue in independent form.

Independent Claim 14

The Office asserts that independent claim 14 has the same scope as originally filed independent claim 1, and that claim 14 is anticipated for the same reasons given for

independent claim 1. The Applicant respectfully disagrees, for the reasons set forth below.

Claim 14 recites, "*a memory control circuit* coupled to the system memory *to provide the at least one memory control signal during an operational state*; and *a second circuit independent of the memory control circuit*, coupled to cause the memory control signal to be at the first value during a power savings state."

Figure 2 of Baweja, upon which the Office relies for its rejection, does not disclose a memory control circuit that provides a control signal during an operational state and a second, independent, circuit that causes the memory control signal to be at the first value during a power savings state. To the contrary, figure 2 of Baweja discloses suspend memory controller 220, which both provides the memory control signal during an operational state and causes the memory control signal to be at the first value during a power savings state. Consequently, Baweja does not disclose a *second circuit independent of the memory control circuit*, as required by independent claim 14.

The Applicant submits, therefore, that Baweja does not teach each and every element of independent claim 14, and cannot support a prima facie rejection of claim 14 under 35 U.S.C. 102(e). Consequently, the Applicant submits that claim 14 is in condition for allowance, and respectfully requests the Office to withdraw its rejection and allow claim 14 to issue.

Independent Claim 21

The Office asserts that independent claim 21 has the same scope as originally filed independent claim 1, and that claim 21 is anticipated for the same reasons given for independent claim 1. The Applicant has amended claim 21 to recite, "second means for controlling the system memory during a power savings state...the second means including means for holding an output terminal at a high impedance during the operational state and means for providing a first logic level through the output terminal during the power savings state." In view of the amendment to claim 21, the applicant submits that claim 21 is allowable.

The Office states, in its rejection of claim 1, that suspend memory controller 220 in figure 2 of Baweja is used to control the memory SDRAM 225 during a power savings state. Baweja does not disclose a means for holding any of the outputs of suspend memory controller 220 at a high impedance during the operational state. It follows, therefore, that Baweja does not disclose, "second means for controlling the system memory during a power savings state...the second means for holding an output terminal at a high impedance during the operational state." as required by amended claim 21.

The Applicant submits, therefore, that Baweja does not teach each and every element of independent claim 21, and cannot support a prima facie rejection of claim 21 under 35 U.S.C. 102(e). Consequently, the Applicant submits that claim 21 is in condition for allowance, and respectfully requests the Office to withdraw its rejection and allow claim 21 to issue.

Independent Claim 26

The Office asserts that independent claim 26 has the same scope as originally filed independent claim 1, and that claim 26 is anticipated for the same reasons given for independent claim 1. The Applicant respectfully disagrees, for the reasons set forth below.

Claim 26 recites, "*controlling at least one memory control signal...from a first region in an integrated circuit...during an operational state; and controlling the...memory control signal from another location in the integrated circuit...during a power savings state in which the first region is not powered...*"

The Office apparently takes the position that in figure 2 of Baweja, first memory controller 210 controls CKE 260 during an operational state, and suspend memory controller 220 controls CKE 260 during a power savings state (see Official Action item 6). Baweja, however, does not disclose that memory controller 210 and suspend memory controller 220 are in separate power regions of an integrated circuit. Claim 26 requires that the memory control signal be controlled "from another location in the integrated circuit...during a power savings state *in which the first region is not powered...*" Since

Baweja does not disclose that the "other location" (presumably suspend memory controller 220) is in a different region *of the integrated circuit* from where the memory control signal is controlled during an operational state (presumably memory controller 210), the Applicant submits that Baweja does not disclose each and every element of claim 26.

Inasmuch as Baweja does not teach each and every element of independent claim 14, it cannot support a prima facie rejection of claim 26 under 35 U.S.C. 102(e). Consequently, the Applicant submits that claim 26 is in condition for allowance, and respectfully requests the Office to withdraw its rejection and allow claim 26 to issue.

Independent Claim 31

The Office asserts that independent claim 31 has the same scope as originally filed independent claim 1, and that claim 31 is anticipated for the same reasons given for independent claim 1. The Applicant has amended claim 31 to include the limitations of original dependent claim 34. Claim 31, as amended, requires that a reset signal be coupled to the second circuit, and that when asserted, the reset signal causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state. In view of the amendments to claim 31, the applicant submits that claim 31 is allowable.

The Office apparently equates the suspend memory controller 220 in figure 2 of Baweja with the second circuit (which operates during a power savings state) recited in claim 31. The Applicant is unable to find in Baweja any reference to a *reset signal* that causes suspend memory controller 220 to "keep the memory control signal at the logic level to maintain the memory in a self refresh state." Consequently, the Applicant submits that Baweja does not teach each and every element of claim 31 as amended.

Inasmuch as Baweja does not teach each and every element of independent claim 31, it cannot support a prima facie rejection of claim 31 under 35 U.S.C. 102(e). Consequently, the Applicant submits that claim 31 is in condition for allowance, and respectfully requests the Office to withdraw its rejection and allow claim 31 to issue.

Dependent Claims 2-13, 15-20, 22, 27-30, and 34

As noted above, dependent claim 8 has been rewritten in independent form, and dependent claim 34 has been incorporated into independent claim 31. As for the remaining dependent claims 2-7, 9-13, 15-20, 22, and 27-30, the Applicant submits that each of the dependent claims depends, either directly or indirectly, from an allowable independent claim. Inasmuch as each of these claims depend from allowable independent claims, the dependent claims are themselves allowable. The Applicant respectfully requests, therefore, that the Office withdraw its rejection of claims 2-13, 15-20, 22, and 27-30 and allow these claims to issue.

IV) Rejection of Claims 32 and 33 under 35 U.S.C. §103(a)

Claims 32 and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Baweja. The Applicant believes that, for the reasons given above, independent claim 31 is in condition for allowance. Inasmuch as claims 32 and 33 depend either directly or indirectly from an allowable independent claim 31, the Applicant submits that claims 32 and 33 are themselves allowable. The Applicant respectfully requests, therefore, that the Office withdraw its rejection of claims 32 and 33, and allow these claims to issue.

V) Rejection of Claims 23-25 Not Specifically Addressed

The Office noted in the current official action that all claims, including claims 23-25, were rejected. The Applicant could not find, however, any specific reasons for the rejection of claims 23, 24 and 25.

Claim 23

Claim 23 depends from claim 21, which for reasons previously discussed, the Applicant believes is allowable. Inasmuch as claim 23 depends from allowable independent claim 21, the Applicant submits that claim 23 is itself allowable.

Claims 24 and 25

Independent claim 24 recites an integrated circuit comprising, "a first output terminal for coupling to a memory control signal that is held at a first logic level to keep a memory in a self refresh state, the integrated circuit responsive to a first operational state of the computer system to *place the output terminal at a high impedance level* and responsive to a power savings state in the computer system to supply the first logic level on the output terminal."

The Applicant respectfully submits that none of the art cited by the examiner teaches or suggests, alone or in combination, a circuit that includes an output terminal for coupling to a memory control signal having a logic level used to keep a memory in a self refresh state, wherein *the circuit places the output terminal at high impedance during one state and then supplies the logic level on the output terminal during another state.* Consequently, the Applicant believes that claim 24 is in condition for allowance, which allowance is respectfully requested.

Inasmuch as dependent claim 25 depends from allowable independent claim 24, the Applicant submits that dependent claim 25 is itself allowable.

Conclusion regarding claims 23, 24, and 25.

For the reasons stated above, the Applicant believes that claims 23, 24, and 25 are in condition for allowance, and respectfully requests allowance of these claims. If the Office maintains its rejection of claims 23, 24, and 25, the Applicant respectfully requests the Office to identify specific references and reasons for its rejection.

CONCLUSION

In summary, claims 1-33 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

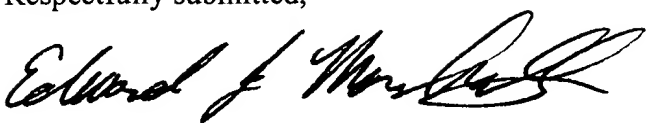
☐ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ facsimile transmitted to the US Patent and Trademark Office.

Edward J. Marshall _____ Date _____

EXPRESS MAIL LABEL: EV335378961US

Respectfully submitted,



Edward J. Marshall, Reg. No. 45,395
Patent Agent
(512) 347-9030
(512) 347-9031 (fax)